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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,690	01/16/2004	Richard L. Black	P/10-658	8450

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EXAMINER	
ROMAN, LUIS ENRIQUE	
ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
05/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/759,690	BLACK, RICHARD L.	
	Examiner	Art Unit	
	Luis Roman	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's amendment filed on 04/04/07 has been entered. Accordingly claims 1-14 have been previously presented. No claims have been amended, cancelled or added new. It also included remarks/arguments.

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Objections

Claims 1-2 & 9-10: are objected to because the following: "***first*** predefined value" (Claims 1 & 9) and "***second*** predefined value" (Claims 2 & 10), these two different values are not supported by the specifications.
For the purpose of further examination the examiner will assume that is the same predefined value for all the claims.
Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C.102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> 102(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 8-11 & 14 are rejected under 35 U.S.C. §102(b) as being anticipated by Ichikawa (US 6285235).

Regarding claims 1 & 9 Ichikawa discloses a gate control circuit for power switching transistor (Fig. 23) wherein the power switching transistor (1) has a control electrode (G) and two main electrodes (C & E), the circuit comprising: a sensing circuit (20, 21, 22, 18a, 18b, 13, 4, 4A, 3E) including a protection switch (3E) for sensing the rate of change of voltage (dv/dt) with respect to time at one of the main electrodes of the power switching transistor (20) and for controlling the protection switch (3E) to remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor if the rate of change (dv/dt) exceeds a predefined value (V_{ref})(Col. 10 line 60 to Col. 11 line 9). For claim 9 the RC circuit is inherently disclosed: the sensing circuit indicated in Fig. 3 by element 20 (dv/dt) comprise a capacitor and a resistor, which is the only way of analogically detect change of voltage. This is the result of the general formula that relates dv/dt and a capacitor C.

$v = 1/C (\int i \times dt) \rightarrow dv/dt = i/C$. This sensing method is also described for example in Skoyles et al. (US 3854779) Col. 12 lines 21-29 & Fig. 8 elements C_{11}, R_{33} & T_{17}.

Regarding claims 2 & 10 Ichikawa discloses the circuit of claim 1.
Ichikawa further teaches the sensing circuit comprises a capacitor coupled to a main electrode of the power switching transistor and a resistor coupled to receive a pulse of current from said capacitor (inherently disclosed<see above>), such that a voltage sensed turns on the protection switch wherein the protection switch is turned on if the voltage sensed exceeds a predefined value (Col. 10 line 60 to Col. 11 line 9). For claim 10 the RC circuit is inherently disclosed (see above).

Regarding claim 3 Ichikawa discloses the circuit of claim 2.
Ichikawa further discloses wherein the protection switch comprises a transistor (Fig. 23 element 3E).

Regarding claims 4 & 11 Ichikawa discloses the circuit of claims above and further teaches wherein the protection switch comprises a bipolar junction transistor (Fig. 23 element 3E).

Regarding claims 8 & 14 Ichikawa discloses the circuit of claims above and further teaches wherein the power switching transistor comprises a field effect transistor (FET) Col. 1 lines 12-17).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a), which forms the basis for all obviousness rejections, set forth in this office action.

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6 & 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Heminger et al. (US 5751052).

Regarding claims 5, 6 & 12 Ichikawa discloses the circuit of claims above but does not disclose wherein the resistor is coupled across the base-emitter junction of the protection transistor and a diode coupled across the base-emitter junction of the protection transistor to discharge the capacitor.

Heminger et al. teaches wherein the resistor is coupled across the base-emitter junction of the protection transistor (Fig. 1 elements 11, 14) and a diode coupled across the base-emitter junction of the protection transistor to discharge the capacitor (Fig. 1 elements 11, 13).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Ichikawa with the teachings of Heminger et al.

because this configuration protects the transistors against leakage and spikes (Heminger et al.<Col. 1 line 61 to Col. 2 line 5>).

Claims 7 & 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Ohura et al. (US 5818281).

Regarding claim 7 & 13 Ichikawa discloses the circuit of claims above but does not teach wherein the protection switch comprises a field effect transistor JFET.

Ohura et al. teaches a protection circuit wherein the protection switch is a FET (Fig. 5 element 2).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Ichikawa with the teachings of Ohura et al. because it allows a higher switching speed (Ohura et al. <Col. 1 lines 12-16>).

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is (571) 272 – 5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.

Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luis E. Román
Patent Examiner
Art Unit 2836

LR/04/25/07

4/27/07

MICHAEL SHERRY
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